

RJK03R4DPA

MOS1 30 V, 20 A, 7.0 mΩ max.

MOS2 30 V, 50 A, 2.3 mΩ max.

Built in SBD Dual N-channel Power MOS FET

High Speed Power Switching

R07DS0888EJ0110

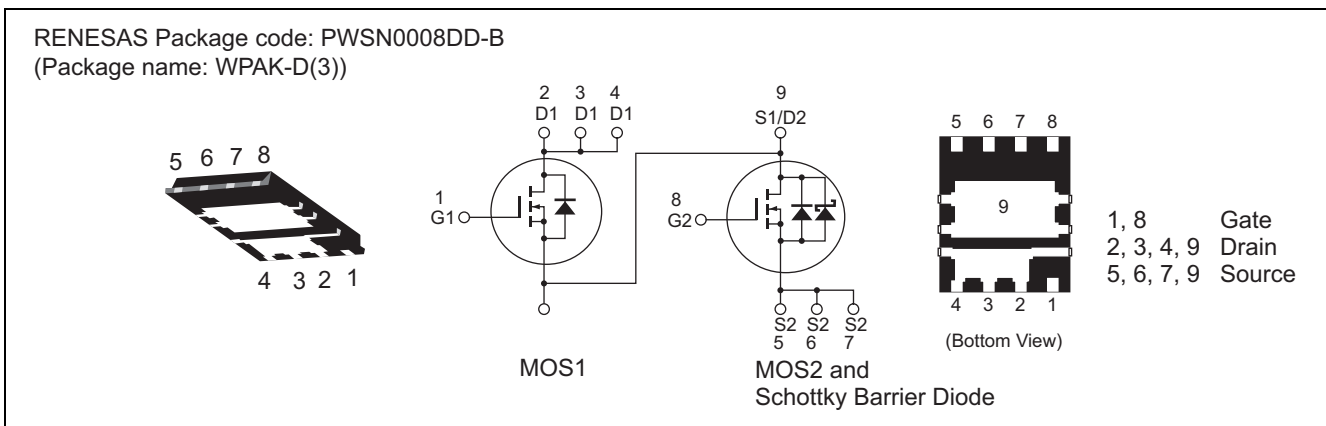
Rev.1.10

Oct 29, 2012

Features

- Low on-resistance
- Capable of 4.5 V gate drive
- High density mounting
- Pb-free
- Halogen-free

Outline



Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings		Unit
		MOS1	MOS2	
Drain to source voltage	V_{DSS}	30	30	V
Gate to source voltage	V_{GSS}	±20	±12	V
Drain current	I_D	20	50	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	80	200	A
Reverse drain current	I_{DR}	20	50	A
Avalanche current	I_{AP} ^{Note 2}	12	22	A
Avalanche energy	E_{AS} ^{Note 2}	14.4	48	mJ
Channel dissipation	P_{ch} ^{Note3}	15	35	W
Channel temperature	T_{ch}	150	150	°C
Storage temperature	T_{stg}	-55 to +150	-55 to +150	°C

- Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1\%$
 2. Value at $T_{ch} = 25^\circ C$, $R_g \geq 50 \Omega$
 3. $T_c = 25^\circ C$

Electrical Characteristics

• MOS1

(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	μA	$V_{DS} = 30 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	5.8	7.0	$\text{m}\Omega$	$I_D = 10 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	8.4	10.9	$\text{m}\Omega$	$I_D = 10 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	35	—	S	$I_D = 10 \text{ A}, V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	1180	1650	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	252	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	90	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.0	2.2	Ω	
Total gate charge	Q_g	—	7.7	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	3.3	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	2.0	—	nC	$I_D = 20 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	3.8	—	ns	$V_{GS} = 10 \text{ V}, I_D = 10 \text{ A}$
Rise time	t_r	—	3.4	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	13.2	—	ns	$R_L = 1.0 \Omega$
Fall time	t_f	—	3.8	—	ns	$R_g = 4.7 \Omega$
Body-drain diode forward voltage	V_{DF}	—	0.83	1.08	V	$I_F = 20 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	9.0	—	ns	$I_F = 20 \text{ A}, V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

Notes: 4. Pulse test

• MOS2

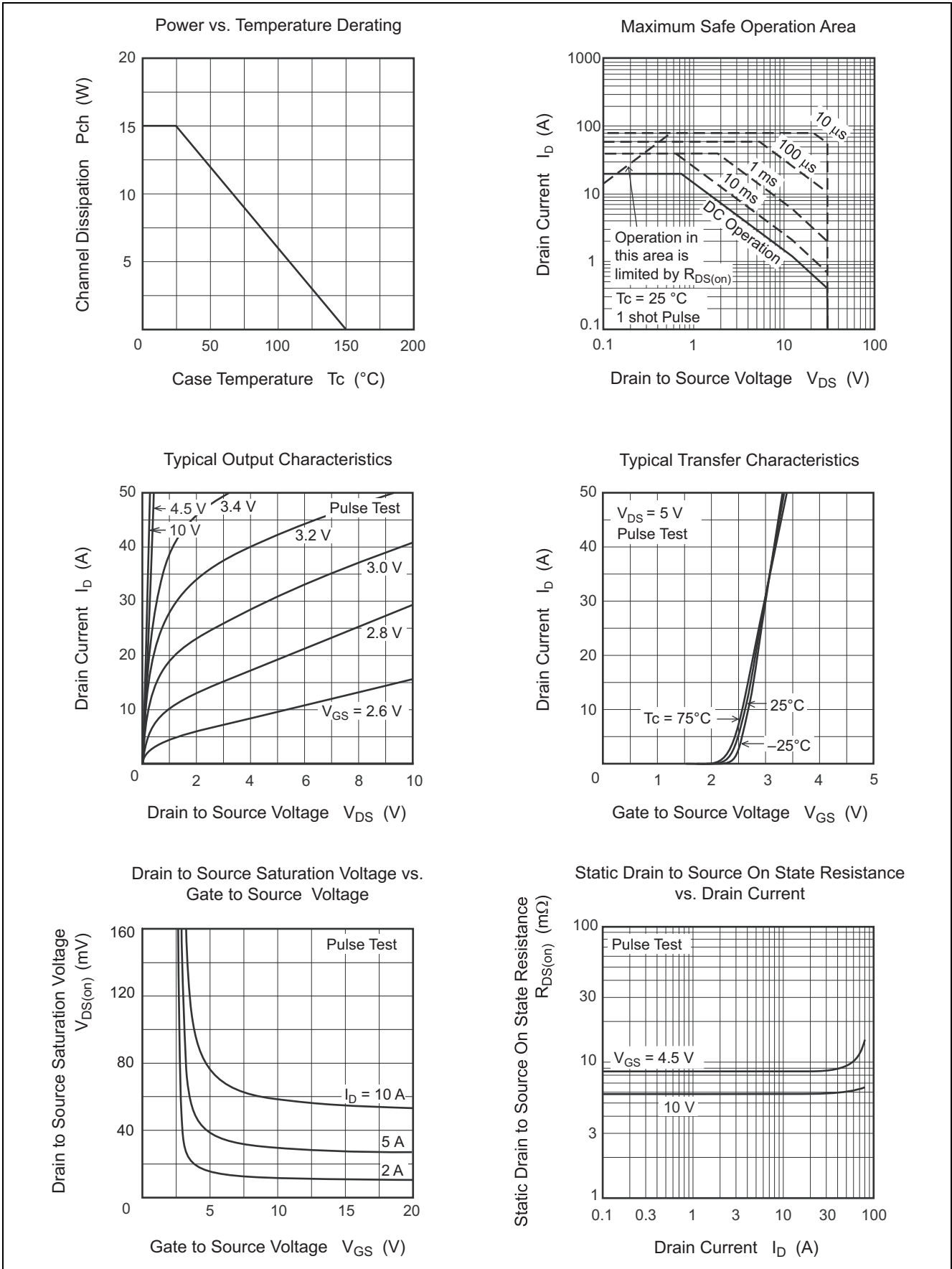
(Ta = 25°C)

Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	30	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{GSS}	—	—	± 0.5	μA	$V_{GS} = \pm 12 \text{ V}, V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	1	mA	$V_{DS} = 24 \text{ V}, V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.2	—	2.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Static drain to source on state resistance	$R_{DS(on)}$	—	1.9	2.3	m Ω	$I_D = 25 \text{ A}, V_{GS} = 8 \text{ V}$ ^{Note4}
	$R_{DS(on)}$	—	2.1	2.8	m Ω	$I_D = 25 \text{ A}, V_{GS} = 4.5 \text{ V}$ ^{Note4}
Forward transfer admittance	$ y_{fs} $	—	133	—	S	$I_D = 25 \text{ A}, V_{DS} = 5 \text{ V}$ ^{Note4}
Input capacitance	C_{iss}	—	6980	9770	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	C_{oss}	—	740	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	C_{rss}	—	450	—	pF	$f = 1 \text{ MHz}$
Gate Resistance	R_g	—	1.0	2.2	Ω	
Total gate charge	Q_g	—	45	—	nC	$V_{DD} = 10 \text{ V}$
Gate to source charge	Q_{gs}	—	19	—	nC	$V_{GS} = 4.5 \text{ V}$
Gate to drain charge	Q_{gd}	—	12	—	nC	$I_D = 50 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	12.4	—	ns	$V_{GS} = 8 \text{ V}, I_D = 25 \text{ A}$
Rise time	t_r	—	6.8	—	ns	$V_{DD} \approx 10 \text{ V}$
Turn-off delay time	$t_{d(off)}$	—	87.2	—	ns	$R_L = 0.4 \Omega$
Fall time	t_f	—	24	—	ns	$R_g = 4.7 \Omega$
Schottky Barrier diode forward voltage	V_F	—	0.40	—	V	$I_F = 2 \text{ A}, V_{GS} = 0$ ^{Note4}
Body-drain diode reverse recovery time	t_{rr}	—	10.0	—	ns	$I_F = 50 \text{ A}, V_{GS} = 0$ $di_F/dt = 500 \text{ A}/\mu\text{s}$

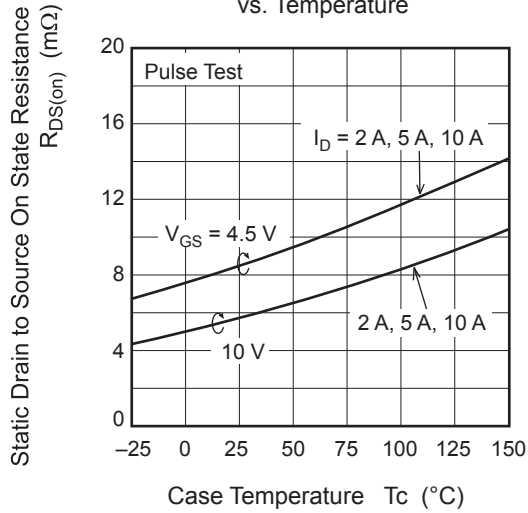
Notes: 4. Pulse

Main Characteristics

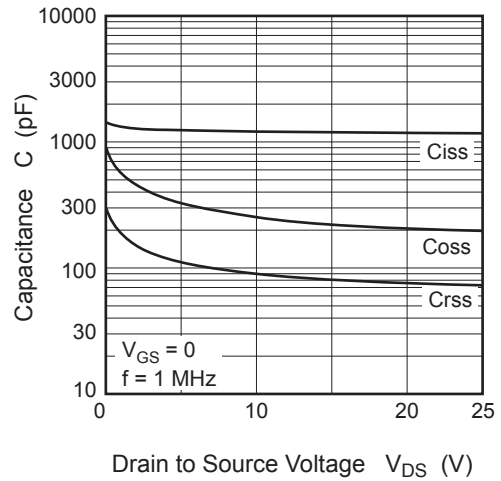
• MOS1



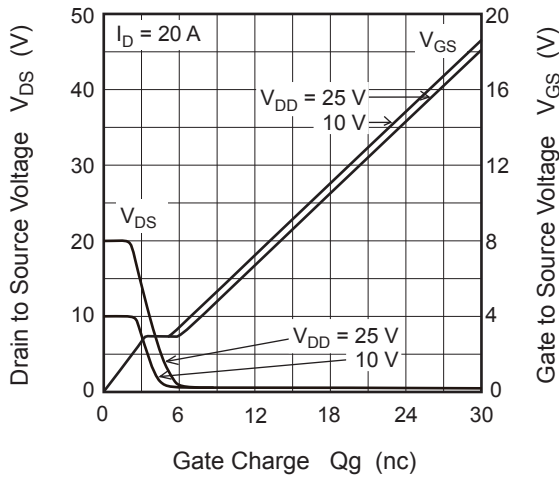
Static Drain to Source On State Resistance vs. Temperature



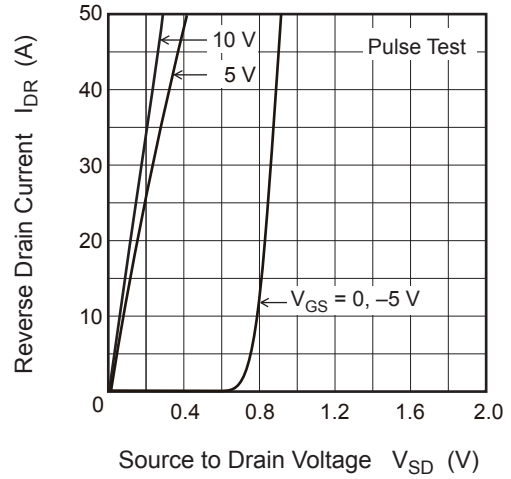
Typical Capacitance vs. Drain to Source Voltage



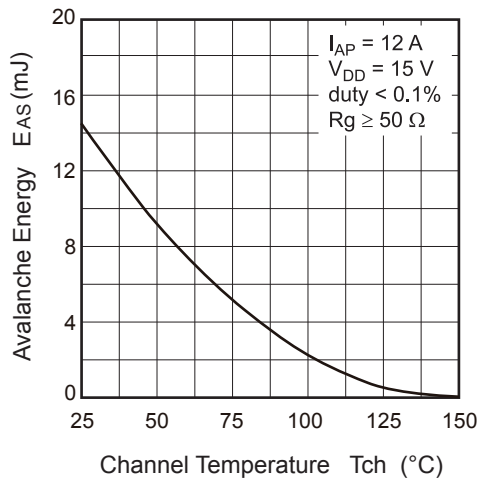
Dynamic Input Characteristics



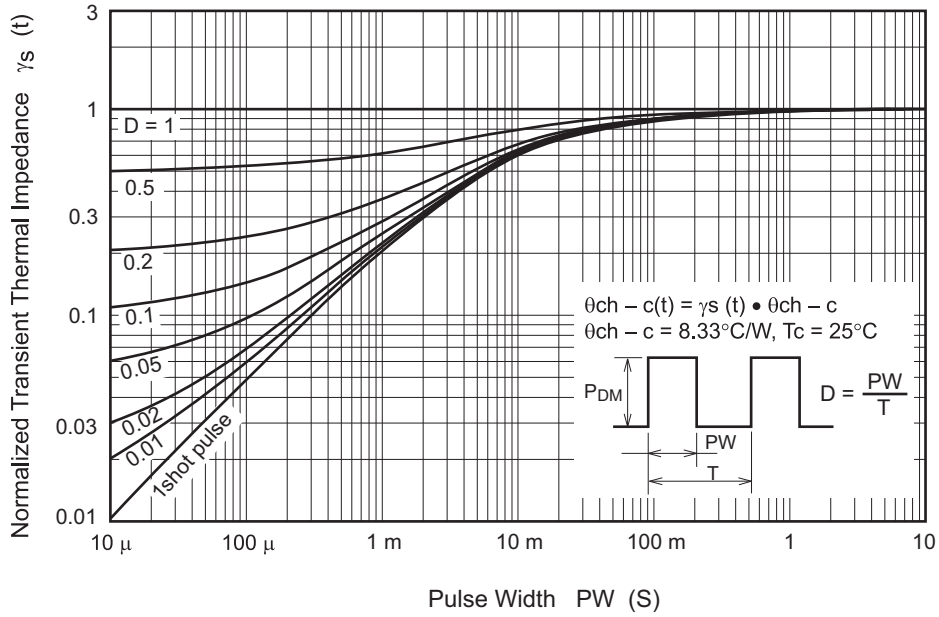
Reverse Drain Current vs. Source to Drain Voltage



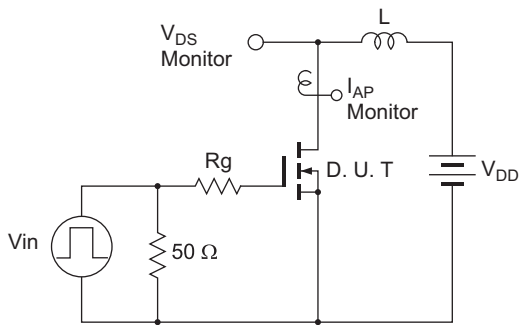
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

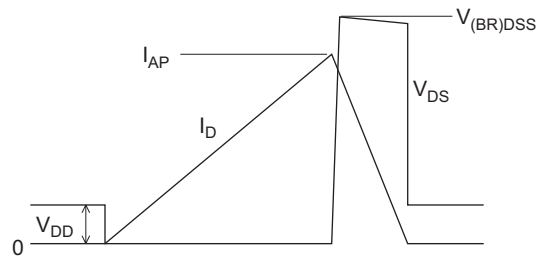


Avalanche Test Circuit

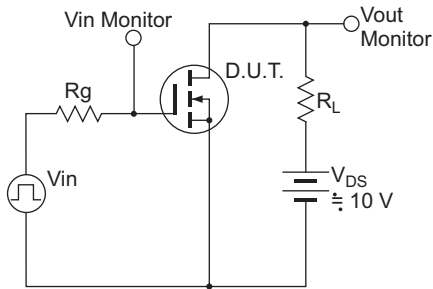


Avalanche Waveform

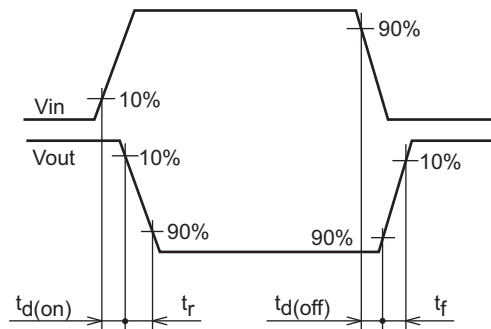
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



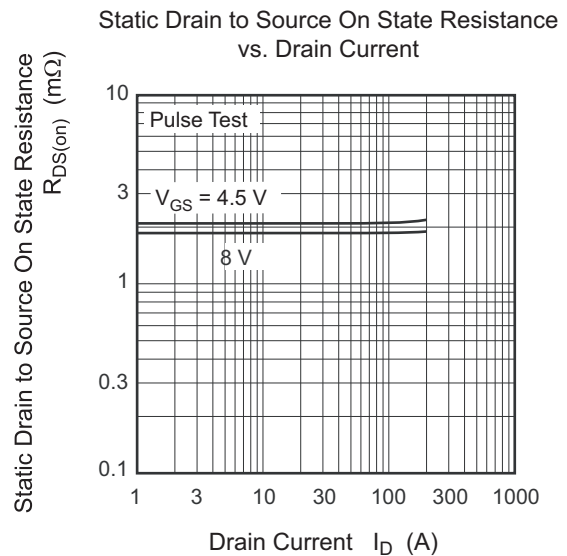
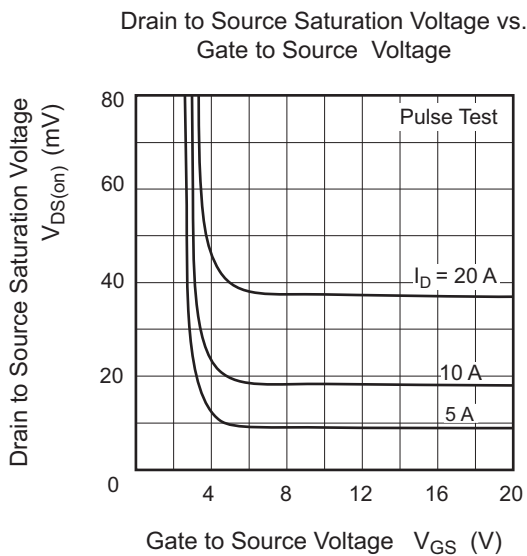
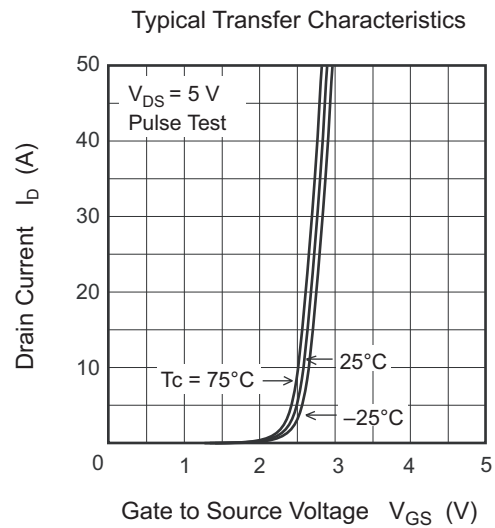
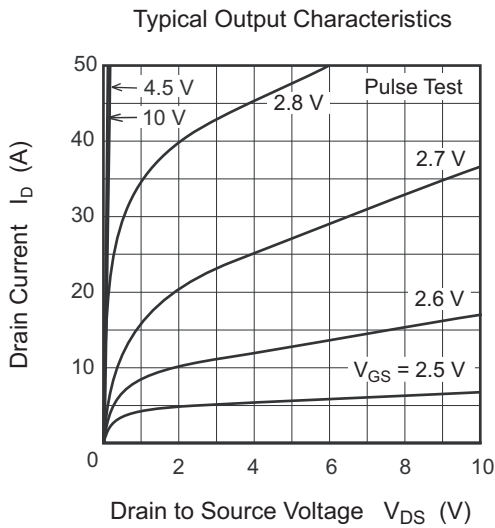
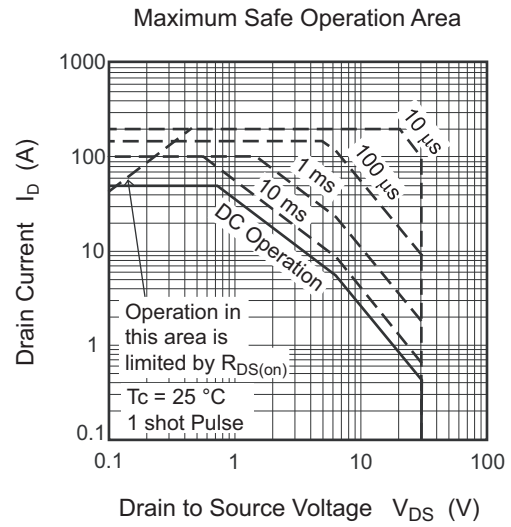
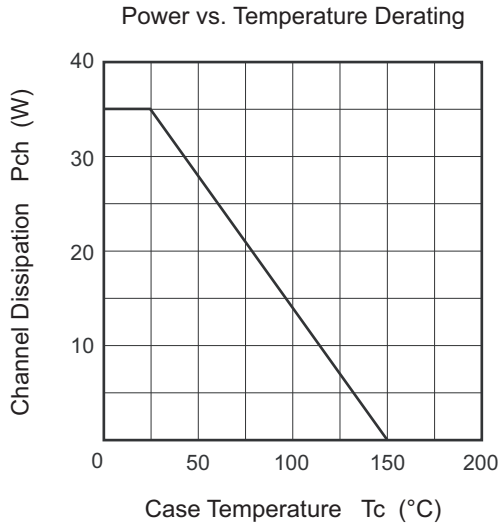
Switching Time Test Circuit



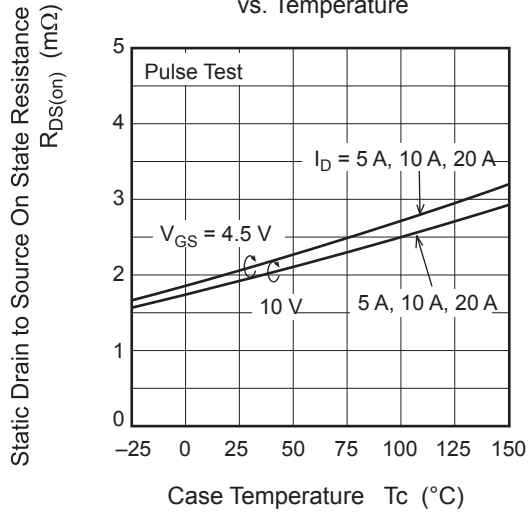
Switching Time Waveform



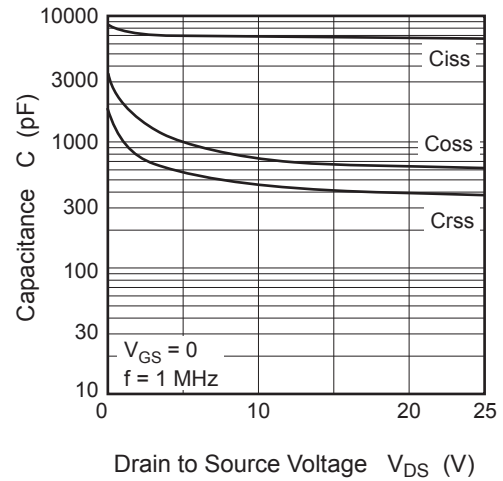
• MOS2



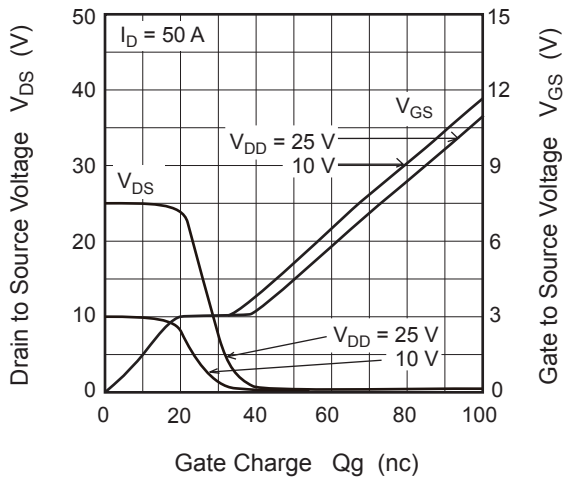
Static Drain to Source On State Resistance vs. Temperature



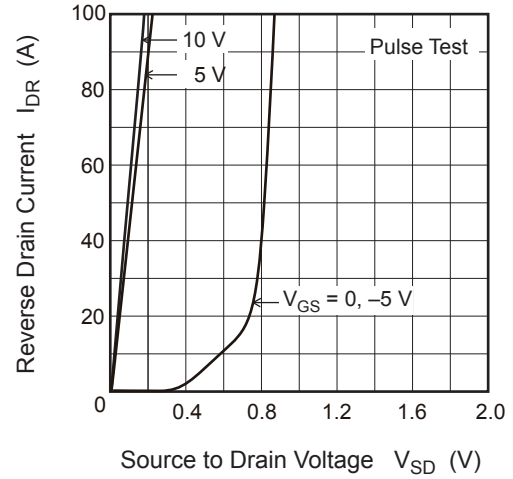
Typical Capacitance vs. Drain to Source Voltage



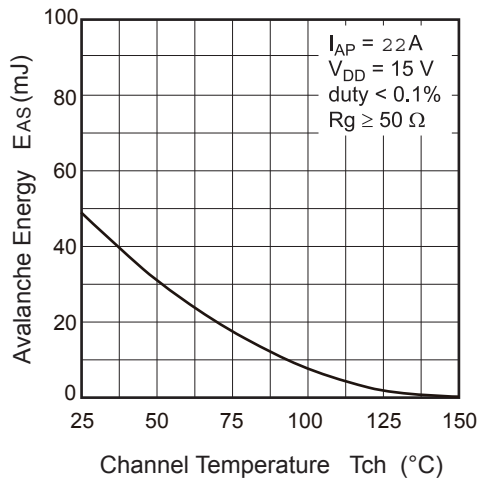
Dynamic Input Characteristics



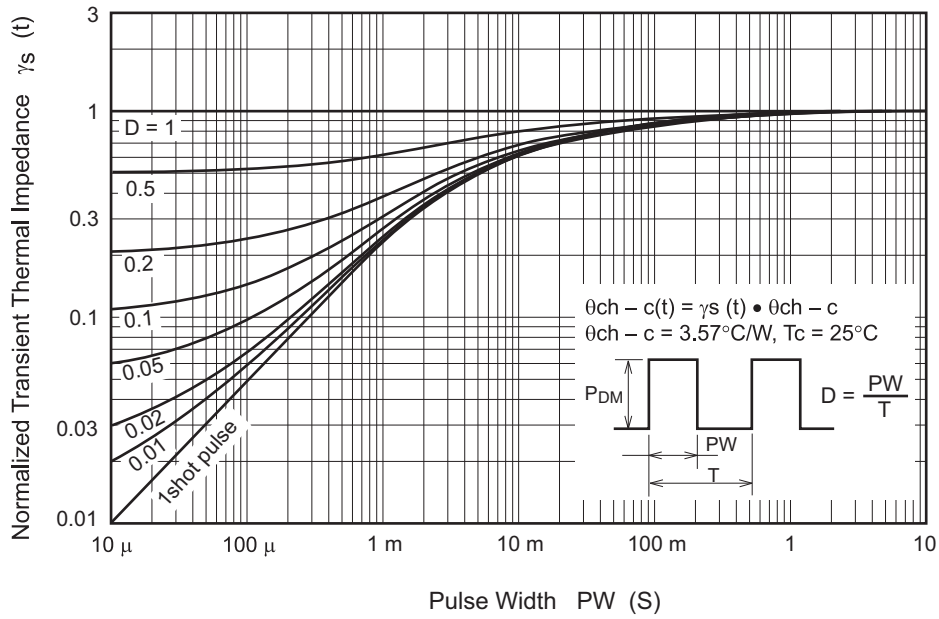
Reverse Drain Current vs. Source to Drain Voltage



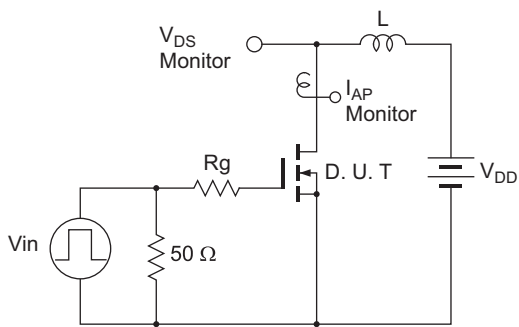
Maximum Avalanche Energy vs. Channel Temperature Derating



Normalized Transient Thermal Impedance vs. Pulse Width

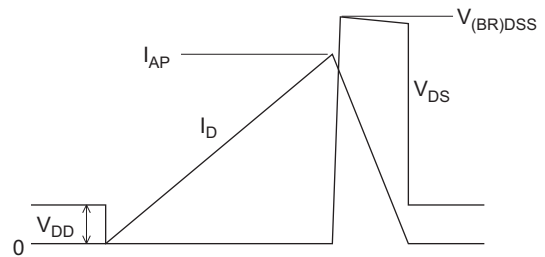


Avalanche Test Circuit

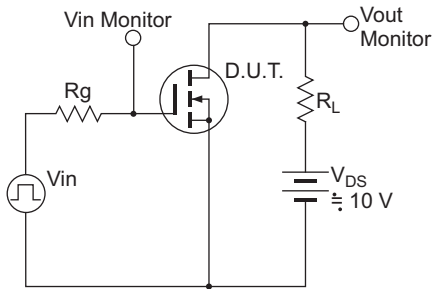


Avalanche Waveform

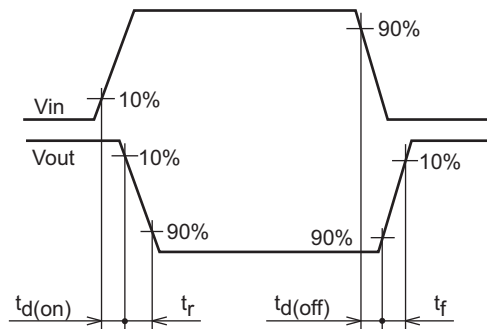
$$E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$



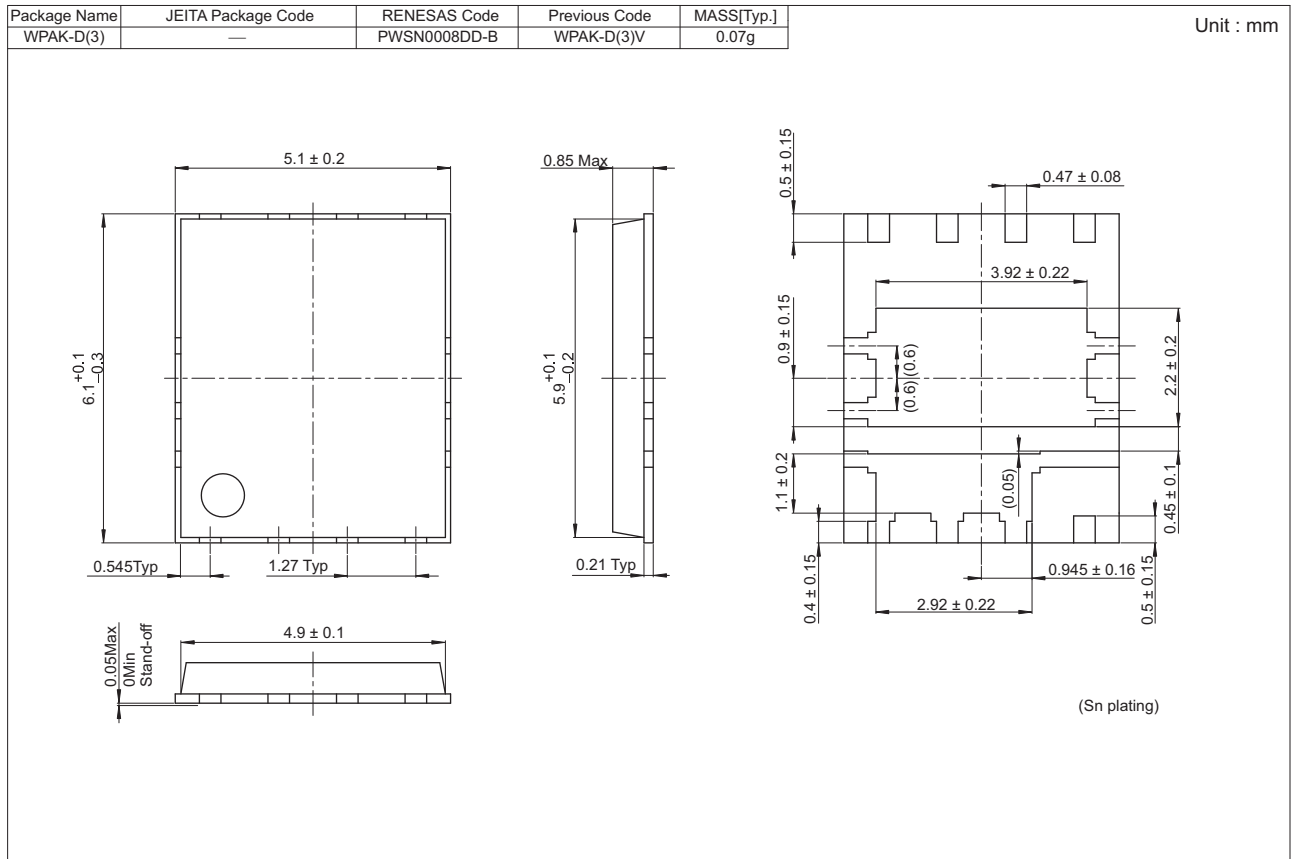
Switching Time Test Circuit



Switching Time Waveform



Package Dimensions



Ordering Information

Orderable Part Number	Quantity	Shipping Container
RJK03R4DPA-00-J5A	3000 pcs	Taping

Note: The symbol of 2nd "-" is occasionally presented as "#".

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